PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Bakir, et al.

Serial No.: 10/647,703

Filed: August 25, 2003

Confirmation No.: 2719

Group Art Unit: 2833

Examiner: To be assigned

Docket No.: 62020-1260

For: DUAL-MODE/FUNCTION OPTICAL AND ELECTRICAL INTERCONNECTS, METHODS OF FABRICATION THEREOF, AND METHODS OF USE THEREOF

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

This information disclosure statement is filed in accordance with 37 C.F.R. §§ 1.56, 1.97, and 1.98, and specifically:

☒ under 37 CFR 1.97(b), or
(within Three months of filing national application; or date of entry of international application; or before mailing date of first office action on the merits; whichever occurs last)

☐ under 37 CFR 1.97(c) together with either a:
- ☐ Statement Under 37 C.F.R. 1.97(e), or
- ☐ a $180.00 fee under 37 CFR 1.17(p), or

(After the CFR 1.97(b) time period, but before the final office action or notice of allowance, whichever occurs first)

☐ under 37 CFR 1.97(d) together with a:
- ☐ Statement under 37 CFR 1.97(e), and
- ☐ a $180.00 petition fee set forth in 37 CFR 1.17(p).

(Filed after final office action or notice of allowance, whichever occurs first, but before payment of the issue fee)

Enclosed is a check in the amount of $. Please charge $ to deposit account . At any time during the pendency of this application, please charge any fees required to Deposit Account 20-0778 pursuant to 37 CFR 1.25. The Commissioner is hereby requested to credit any overpayment to Deposit Account No. 20-0778.

☒ Applicant(s) submit herewith *Form PTO 1449A - Information Disclosure Statement by Applicant* together with copies (where required) of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may or may not be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56. As required by 37 C.F.R. §1.98(a), a legible copy of each document is provided.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individual(s) designated in 37 CFR 1.56(c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on the form PTO 1449 and is enclosed herewith.

The following rights are reserved by the Applicant(s): the right to establish the patentability of the claimed invention over any of the listed documents should they be applied as reference, and/or the right to prove that some of these documents may not be prior art, and/or the right to prove that some of these documents may not be enabling for the teachings they purport to offer.

This statement should not be construed as a representation that an exhaustive search has been made, or that information more material to the examination of the present application does not exist. Any statements or identifications regarding the relevance of any portion(s) of cited references should not be construed as a representation that the most relevant portion(s) have been identified, and the absence of such statements or identifications should not be construed as representations that there are no relevant portion(s). The Examiner is specifically requested not to rely solely on the materials submitted herewith. The Examiner is requested to conduct an independent and thorough review of the documents, and to form independent opinions as to their significance.

It is requested that the information disclosed herein be made of record in this application and that the Examiner initial and return a copy of the enclosed PTO-1449 to indicate the documents have been considered.

Respectfully Submitted,

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

By: _____

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CERTIFIED MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as **"First Class Mail,"** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on January 20, 2004.

_____
Jo Bryan

Form PTO-1449

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

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62020-1260	**10/647,703**
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Filing Date: **8/25/03**	Group: **2833**

U.S. PATENT DOCUMENTS

Examiner Initials	Item	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	A	4,380,365	4/19/83	Gross	350	96.18	5/23/79
	B	5,046,800	9/10/91	Blyler, Jr., et al.	385	131	10/9/90
	C	5,130,356	7/14/92	Feuerherd, et al.	524	96	2/1/90
	D	5,302,656	4/12/94	Kohara, et al.	524	579	4/10/91
	E	5,359,208	10/25/94	Katsuki, et al.	257	82	2/26/93
	F	5,454,196	7/18/95	Ohkawa, et al.	522	100	7/1/94
	G	5,462,995	10/31/95	Hosaka, et al.	525	332.1	6/9/92
	H	5,581,414	12/3/96	Snyder	359	819	2/22/93
	I	5,896,479	4/20/99	Vladic	385	59	4/9/97
	J	6,022,498	2/8/00	Buazza, et al.	264	1.38	4/19/96
	K	6,039,897	3/21/00	Lochhead, et al.	264	1.24	8/28/97

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, etc.)*

	L	Chen, et al.; Fully Embedded Board-Level Guided-Wave Optoelectronic Interconnects; June, 2000; Proceedings of IEEE, Vol. 88, No. 6; pp 780-793
	M	Wiesmann, et al.; Singlemode Polymer Waveguides for Optical Backplanes; December 5, 1996; Electronics Letters, Vol. 32, No. 25; pp 2329-2330
	N	Barry, et al.; Highly Efficient Coupling Between Single-Mode Fiber and Polymer Optical Waveguides; August, 1997; IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 20, No. 3; pp 225-228
	O	Lee, et al.; Fabrication of Polymeric Large-Core Waveguides for Optical Interconnects Using a Rubber Molding Process; January, 2000; IEEE Photonics Technology Letters, Vol. 12, No. 1; pp 62-64
	P	Schmeider, et al.; Electro-Optical Printed Circuit Board (EOPCB); 2000 Electronic Components and Technoogy Conference; pp 749-753
	Q	Mederer, et al.; 3Gb/s Data Transmission With GaAs VCSELs Over PCB Integrated Polymer Waveguides; September, 2001; IEEE Photonics Technology Letters, Vol. 13, No. 9; pp 1032-1034

* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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	R	6,156,394	12/5/00	Schultz Yamasaki, et al.	427	536	4/17/98
	S	6,206,673	3/27/01	Lipscomb, et al.	425	174.4	5/30/95
	T	6,253,004	6/26/01	Lee, et al.	385	31	7/9/99
	U	6,259,567	7/10/01	Brown, et al.	359	668	11/23/98
	V	6,262,414	7/17/01	Mitsuhashi	250	216	7/27/99
	W	6,272,275	8/7/01	Cortright, et al.	385	129	6/25/99
	X	6,281,508	8/28/01	Lee, et al.	250	396	2/8/99
	Y	6,432,328	8/13/02	Hamanaka, et al.	264	1.36	1/10/01
	Z	6,500,603	12/31/02	Shioda	430	321	11/9/00
	AA						
	BB						

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		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, etc.)*

	CC	Schröder, et al.; Polymer Optical Interconnects for PCB; 2001; Session 13: Photonic Polymers II; pp 337-343
	DD	Glukh, et al.; High performance Polymeric Materials for Waveguide Applications; August, 2000; SPIE - The International Society for Optical Engineering, inear, Nonlinear, and Power Limiting Organics, San Diego, Volume 4106; pp 1-11
	EE	Liu, et al.; Plastic VCSEL Array Packaging and High Density Polymer Waveguides for Board and Backplane Optical Interconnect; 1998; Electronic Components and Technology Conference; pp 999-1005
	FF	Bakir, et al.; Sea of Dual Mode Polymer Pillar I/O Interconnections for Gigascale Integration; 2003; IEEE International Solid State Circuits Conference; 8 pages
	GG	Beuret, et al.; Microfabrication of 3D Multidirectional Inclined Structure by UV lithography and Electroplating; Micro Electro Mechanical Systems, 1994, MEMS'94, Proceedings, IEEE Workshop on January 25-28, 1994; pp 81-85
	HH	Wang, et al.; Studies on A Novel Flip-Chip Interconnect Structure-Pillar Bump; Electronic Components and Technology Conference, 2001, Proceedings, 51st, 29 May-1, June 2001; pp 945-949

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U.S. PATENT DOCUMENTS

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	II						
	JJ						
	KK						

FOREIGN PATENT DOCUMENTS

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							Yes	No

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, etc.)*

	LL	Bakir, et al.; Sea of Polymer Pillars: Dual-Mode Electrical Optical Input/Output Interconnections; in Proc. of Int. Interconnect Technology Conference; pp. 77-79; 2003
	MM	Bakir, et al.; Sea of Polymer Pillars: Compliant Wafer-Level Electrical-Optical Chip I/O Interconnections; IEEE Photonics Technology Letters, Vol. 15, No. 11, November 2003; pp 1567-1569
	NN	Bakir, et al.; Optical Transmission of Polymer Pillars for Chip I/O Optical Interconnections; IEEE Photonics Technology Letters, Vol. 16, No. 1, January 2004; pp 117-119
	OO	Chandrasekhar, et al.; Modeling and Characterization of the Polymer Stud Grid Array (PSGA) Package: Electrical, Thermal and Thermo-Mechanical Qualification; IEEE Transactions on Electronics Packaging Manufacturing, Vol. 26, No. 1, January 2003; pp 54-67

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